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06CS81

Eighth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Advanced Computer Architecture

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Define computers architecture. Illustrate seven dimensions of an ISA? (10 Marks)
b. Explain in brief, measuring, reporting and summarizing performance of computer. (10 Marks)
- 2 a. What are the major hurdles of pipelining? Illustrate the branch hazard in detail. (10 Marks)
b. Explain five ways of classifying exception in a computer system. (10 Marks)
- 3 a. What are the techniques used to reduce branch costs? Explain both static and dynamic branch. (10 Marks)
b. What is the drawback of 1-bit dynamic branch prediction method? Clearly state how it is overcome in 2-bit prediction. Give the state transition diagram of 2-bit predictor. (10 Marks)
- 4 a. Explain the basic VLIW approach for exploiting ILP using multiple issues. (10 Marks)
b. What are the key issues in implementing advanced speculation techniques? Explain then in detail. (10 Marks)

PART – B

- 5 a. Explain the basic schemes for informing coherence in a shared memory multiprocessor system. (10 Marks)
b. Explain the directory based coherence for a distributed memory multiprocessor system. (10 Marks)
- 6 a. Explain in brief the types of basic cache optimization. (10 Marks)
b. With a neat diagram, explain organization of data cache in the opteron microprocessor. (10 Marks)
- 7 a. Which are the major categories of the advanced optimization of cache performance? Explain any one in detail. (10 Marks)
b. Explain in detail the architecture support for protective processes from each other via virtual memory. (10 Marks)
- 8 a. Explain in detail the H/w support for preserving exception behaviour during speculation. (10 Marks)
b. Explain the prediction and speculation support provided in IA-64. (10 Marks)

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